MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2019/2020

EEE4166 – DIGITAL INTEGRATED CIRCUIT

(All sections / Groups)

22 OCTOBER 2019
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 6 pages with 4 questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\phi_T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69\, R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) Figure Q1 shows a series diode circuit with voltage supply, V1 = 5 V and the resistor, R1 = 2 kΩ. Using the simple diode model, with V_D = 0.7 V,

(i) Determine the voltage drop on resistor, V_{R1} and current, I_D of the circuit. [4 marks]

(ii) At a temperature 27^{0}C, with reverse saturation current, I_S = 5 fA and the thermal voltage, V_T or ϕ_T = 26 mV, calculate the new I_D value. [2 marks]

(iii) Describe the forward-biased state of the p-n junction diode, emphasizing on the holes and electrons movement. [4 marks]

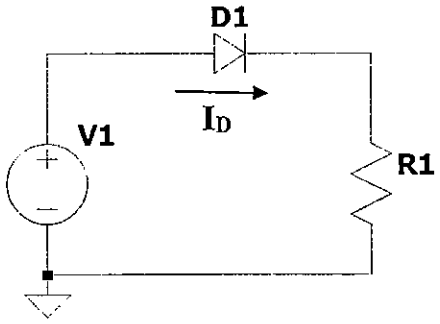

Figure Q1

(b) In a generic 0.18 μm CMOS process, the parameter values for a minimum sized NMOS transistor are given as threshold voltage, V_{T0} = 0.4 V, $-2\varphi_F$ = 0.8 V, body effect coefficient, γ = 0.4 $\sqrt{V}$ and k_n' = 115 μA/V^2.

(i) An NMOS transistor has aspect ratio W/L = 3/2 is operating with V_{SB} = 1.6 V, V_{GS} = 2 V and V_{DS} = 3 V. Determine the actual threshold voltage, V_{th}. Then determine the mode of operation and the drain current, I_D for this transistor. [8 marks]

(ii) Calculate the drain current, I_D for a similar NMOS transistor which has the size of W/L = 20. [2 marks]

(c) An actual MOS device has deviated from its behavior of an ideal MOS transistor which gives several second-order effects. Explain TWO of the secondary effects and propose a solution for each effect. [5 marks]

Continued...

Question 2

(a) Consider a static CMOS inverter as shown in Figure Q2 (a) below.

(i) Describe TWO important properties of a static CMOS inverter. [4 marks]

(ii) In Figure Q2 (b) below, determine the operating regions (linear, saturation or cutoff) for both transistors (PMOS and NMOS) at part P2, P3 and P4. [6 marks]

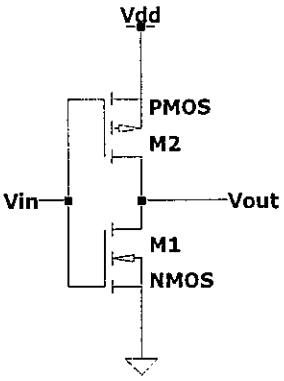

Figure Q2 (a)

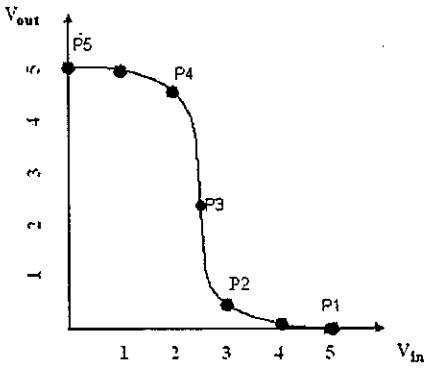

Figure Q2 (b)

(b) Given the function Y below:

$$Y = (A.\bar{B}) + C$$

(i) Design a static CMOS gate realization of this function Y with minimum transistor count. The input and inverted input ports are available for implementation. [6 marks]

(ii) From the design in Part (i), size the W/L ratios of the transistors so that the output resistance is the same as that of an inverter with $(W/L)_{NMOS} = 1$ and $(W/L)_{PMOS} = 4$. [4 marks]

(c) A relaxation oscillator is an astable, nonlinear electronic oscillator circuit that produces its repetitive behavior from the charging of a capacitor. Describe the operation of a relaxation oscillator, including its circuit diagram. [5 marks]

Continued...

Question 3

(a) Referring to Figure Q3(a) below, a basic TTL NAND circuit is shown.

(i) Assuming the transistor has $V_{BE(on)}$ = 0.7 V, $V_{BE(sat)}$ = 0.8 V, $V_{CE(sat)}$ = 0.1 V with V_{CC} = 5 V, $R_1 = R_C$ = 3.5 kΩ. If either or both of the inputs to Q1 are in a low state (0.1 V), calculate the voltages v_{B1}, v_o and current i_{B1}. [6 marks]

(ii) Discuss THREE advantages of TTL gate compared to basic bipolar transistor. [6 marks]

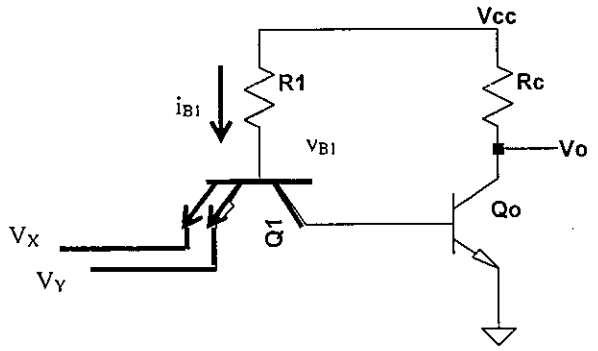

Figure Q3(a)

(b) A BiCMOS inverter circuit is shown in Figure Q3(b) below.

(i) Describe the operation of the BiCMOS inverter circuit when the input voltage, v_I applied is HIGH (at V_{OH}). [8 marks]

(ii) Assuming that the inverter has V_{DD} = 3 V, V_{BE} = 0.7 V, R_1 = 2 kΩ, R_2 = 6 kΩ, C_L = 10 pF and β =100. As for CMOS, the threshold voltages V_{tp} = -0.5 V, V_{tn} = 0.5 V and K_N = 120 μA/V^2. Assume V_{OL} = 0 V and V_{OH} = 3 V. Calculate t_{pHL} and t_{pd}. [5 marks]

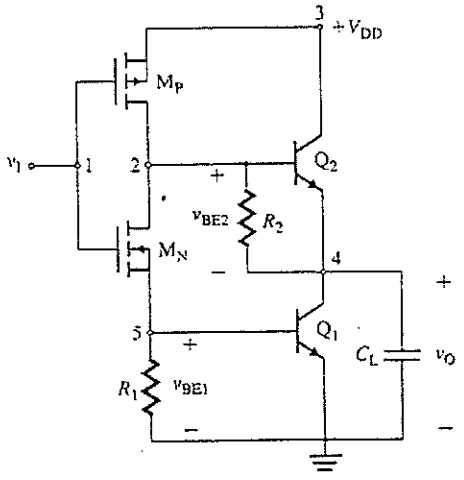

Figure Q3(b)

Continued...

Question 4

(a) For the following function:

$$F = \overline{A.B} + C$$

(i) Implement the F function with static CMOS gates.

[8 marks]

(ii) Based on the circuit implemented in Part (i), sketch a truth table and determine the dynamic power consumption, P_{dyn} of the circuit, assuming that the load capacitance, C_L = 10 fF, voltage supply; V_{DD} = 3 V and clock frequency, f_{clk} = 20 MHz. Assume that the input signals are random.

[9 marks]

(b) Figure Q4 shows the Normalized Power Dissipation with scaling of the gate length and technology nodes (Year).

(i) Based on this Figure Q4, comment on the graph. [4 marks]

(ii) Propose TWO methods to reduce and minimize the power dissipation in a circuit. [4 marks]

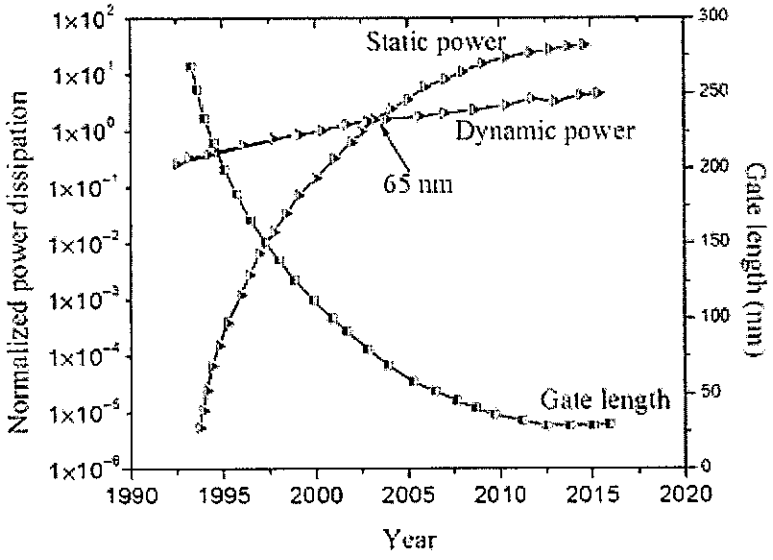

Figure Q4

End of Paper